SEMICONDUCTOR MEMORY DEVICE HAVING A PLUG CONTACTED TO A CAPACITOR ELECTRODE AND METHOD FOR FABRICATING THE CAPACITOR

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method for fabricating a semiconductor memory device; and more particularly, to a method for fabricating a capacitor of a semiconductor memory device.

Description of the Prior Art

A DRAM (Dynamic Random Access Memory) cell is a semiconductor memory device typically comprising of one transistor and one capacitor, in which one bit of data is stored in a cell by using an electric charge. A capacitor comprises of a lower electrode, a dielectric layer, and an upper electrode. One electrode of the capacitor is connected to the source/drain junction of the transistor. Another electrode of the capacitor is connected to a reference voltage line.

Advances in computer applications have increased the demand for higher capacity memory chips. By decreasing the size of the memory cells, more memory cells can be packed into an integrated circuit.

The capacitance of a capacitor is proportional to the surface area of the electrodes and a dielectric constant of a dielectric layer. As the area of the memory cell has decreased, the capacitance of the capacitor tends to decrease. This lowers the performance of the memory cells.

In order to increase the density of the memory cells, stacked capacitors have been proposed. Stacked capacitors are formed by partially stacking the storage electrode over the transistor and over the bit/word line, thereby effectively reducing the area used for each memory cell.

A plug is used to connect the lower electrode of the capacitor with the source/drain junction of the transistor.

A method for fabricating a capacitor of a semiconductor memory device according to the conventional method is described by referring to FIG. 1A to FIG. 1C.

As shown in FIG. 1A, an insulating layer 15 is formed over a semiconductor substrate 10, an isolation layer 11, such as field oxide layer, and a transistor comprising a gate insulating layer 12, a gate electrode 13 and the source/drain junctions 14. Thereafter, a plug 16 is formed in the interlayer insulating layer. The plug 16 is composed of a polysilicon layer 16A, an ohmic contact layer 16B and a diffusion barrier layer 16C formed in a contact hole, exposing

one of a source/drain junctions 14.

As shown in FIG. 1B, a lower electrode 17 is formed on the diffusion barrier layer 16C by depositing and patterning a first conductive layer. The diffusion barrier layer 16C may be exposed during the formation of the lower electrode 17 because of a mask misalignment. The mask misalignment frequently occurs in the manufacturing process of the highly integrated device.

As shown in FIG. 1C, a dielectric layer 18 is formed on the lower electrode 17 and an upper electrode 19 is formed on the dielectric layer 18. The dielectric layer 18 is formed with a material exhibiting a very high dielectric constant, such as Barium Strontium Titanate ($BaSrTiO_3$, hereafter abbreviated BST), to increase the capacitance in a highly integrated device.

The present invention relates to a method for fabricating a semiconductor memory device; and more particularly, to a method for fabricating a capacitor of a semiconductor memory device.

An electro plating technique is used to form the lower electrode without an etching process.

A method for fabricating a capacitor of a semiconductor memory device according to a second conventional method, by

using the electro plating technique, is described by referring to FIG. 2A to FIG. 2E.

As shown in FIG. 2A, an insulating layer 15 is formed over a semiconductor substrate 10, an isolation layer 11, such as a field oxide layer, and a transistor comprising a gate insulating layer 12, a gate electrode 13 and source/drain junctions 14. Thereafter, a plug 16 is formed in the insulating layer. The plug 16 is composed of a polysilicon layer 16A, an ohmic contact layer 16B and a diffusion barrier layer 16C formed in a contact hole, exposing one of the source/drain junctions 14.

As shown in FIG. 2B, a seed layer 21 is formed on the insulating layer 15 and the plug 16, thereafter a glue layer 22 and a sacrificial layer 23 are stacked, one by one, on the seed layer 21.

As shown in FIG. 2C, the sacrificial layer 23 and the glue layer 22 are selectively etched to form an opening exposing the seed layer 21. A lower electrode 17 is formed on the seed layer 21 in the opening.

As shown in FIG. 2D, the sacrificial layer 23, the glue layer 22 and the seed layer 21 are removed to separate the neighboring lower electrodes 17.

As shown in FIG. 2E, a dielectric layer 18 is deposited on

the lower electrode 17 and the insulating layer 15. Thereafter, an upper electrode 19 is formed on the dielectric layer 18.

In the mentioned process of the second conventional method, the diffusion barrier layer 16C of the plug 16 may be exposed after removing the seed layer 21 when mask misalignment has occurred in the process for forming the opening.

According to the stated conventional method, the exposed part of the diffusion barrier layer 16C of the plug 16 is contacted to the dielectric layer 18.

There are several problems caused by the contact between the diffusion layer 16C and the dielectric layer 18. One problem is that the diffusion barrier layer 16C is oxidized during the process for forming the dielectric layer 18, because the dielectric layer 18, (such as the BST layer), is formed under an oxygen gas atmosphere and at a high temperature. The oxidized part of the diffusion barrier layer 16C, exhibiting low dielectric constant, plays the role of the dielectric layer of the capacitor, thereby the capacitance of the capacitor is reduced. The other problem is that the work function difference, between the diffusion barrier 16C and the dielectric layer 18, is low. Thus, the leakage current is increased, because of the low Schottky barrier height.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a semiconductor memory device and a fabrication method capable of preventing contact between a dielectric layer of a capacitor and a diffusion barrier of a plug.

It is, therefore, another object of the present invention to provide a semiconductor memory device and a fabrication method capable of preventing a lowering of the capacitance of the capacitor and an increase of the leakage current between the lower electrode of the capacitor and a diffusion barrier of a plug.

In accordance with an aspect of the present invention, there is provided a semiconductor memory device, comprising a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein source/drain junctions are formed in the semiconductor substrate.

An interlayer insulating layer is formed over the semiconductor substrate and a plug is formed in the interlayer insulating layer. The plug comprises a diffusion barrier layer and a seed layer for a electro plating. A lower electrode of the capacitor is contacted to the seed layer. A dielectric layer is formed on the lower electrode and an upper electrode

is formed on the dielectric layer.

In accordance with another aspect of the present invention, there is provided a method for fabricating semiconductor memory device. The method includes the steps of providing a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein source/drain junctions are formed in the semiconductor substrate, and forming an interlayer insulating layer over the semiconductor substrate. The interlayer insulating layer is etched to form a contact hole. A plug is formed in the contact hole. The plug comprises a diffusion barrier layer and a seed layer for electro plating. A lower electrode of a capacitor is formed and is contacted to the seed layer by using the electro plating technique. Also, a dielectric layer of the capacitor is formed on the lower electrode and an upper electrode of the capacitor is formed on the dielectric layer.

In accordance with still further aspect of the present invention, there is a method for fabricating semiconductor memory device. The method includes the steps of providing a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein a plurality of source/drain junctions are formed in the semiconductor substrate and forming an interlayer insulating layer over the

semiconductor substrate. The interlayer insulating layer is etched to form a contact hole. A plug is formed in the contact hole, wherein the plug comprises a diffusion barrier layer and a seed layer for electro plating. A glue layer is formed on the seed layer and the interlayer insulating layer. A sacrificial layer is formed on glue layer. The sacrificial layer and the glue layer are etched to form an opening defining a region of a lower electrode of a capacitor. The lower electrode is formed on the seed layer in the opening, by using the electro plating technique. The sacrificial layer and the glue layer are removed. A dielectric layer of the capacitor is formed on the lower electrode and an upper electrode of the capacitor is formed on the dielectric layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects and features of the present invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

FIG. 1A to FIG. 1C are cross sectional views showing a method for fabricating a semiconductor memory device according to a first conventional method.

FIG. 2A to FIG. 2E are cross sectional views showing a

method for fabricating a semiconductor memory device according to a second conventional method.

FIG. 3A to FIG. 3I are cross sectional views showing a method for fabricating a capacitor of a semiconductor device according to the present invention.

DESCRIPTION OF THE INVENTION

Hereinafter, a semiconductor memory device fabrication method according to the present invention will be described in detail referring to the accompanying drawings.

As shown in FIG. 3A, a conducting layer 31 is formed over a semiconductor substrate 30. A determined lower structure (not shown), comprises an isolation layer, such as a field oxide layer, a transistor including a gate insulating layer, a gate electrode and the source/drain junctions. Thereafter, an interlayer insulating layer, composed of a first insulating layer 32 and a second insulting layer 33, is formed on the conducting layer 31.

The conducting layer 31 is used as an electrode for forming a lower electrode of a capacitor, by using electro plating technique. In the present invention, a doped polysilicon layer is deposited and a thermal treatment process is performed to

activate impurities in the doped polysilicon layer, whereby the conducting layer 31 is formed.

The process for forming the conducting layer 31 may be omitted, in this case, and the semiconductor substrate 30 may be used as the electrode for forming a lower electrode of a capacitor. The second insulating layer 33, playing as an antireflection layer, is formed with a material of which etching is selectivity higher than the first insulating layer 32. In the present invention, the first insulating layer 32 is formed by depositing a silicon oxide layer to a thickness of 3000 - 8000 Å, and the second insulating layer 33 is formed by depositing a silicon nitride layer to a thickness of 300 to 1000 Å.

As shown in FIG. 3B, the second insulating layer 33 and the first insulating layer 32 are etched to form a contact hole exposing the conducting layer 31. One of the source/drain junctions (not shown) formed in the semiconductor substrate 30 may be exposed by the contact hole, if the conducting layer 31 is not formed.

And then, a polysilicon layer 34A, for forming a plug, is deposited to a thickness of 500 - 3000 Å on the second insulating layer 33 and in the contact hole. Thereafter, an etching process is performed to expose the surface of the second

insulting layer 33 and to remove a part of the polysilicon layer 34A in the contact hole. Thereby, the height difference between the surface of the second insulating layer 33 and the surface of the polysilicon layer 34A becomes 500 to 1500 Å.

As shown in FIG. 3C, an ohmic contact layer 34B and a diffusion barrier layer 34C are formed, one by one, on the polysilicon layer 34A. Subsequently, a chemical mechanical polishing (hereafter, abbreviated CMP) process is performed until the surface of the second insulating layer 33 is exposed. In the present invention, the ohmic contact layer 34B is formed with $TiSi_x$ and the diffusion barrier layer 34C is formed with TiN, TiSiN, TiAlN, TaSiN, TaAlN, IrO_2 or RuO_2. For forming the $TiSi_x$, a Ti layer is deposited, an annealing process is performed for a reaction between Ti atom in the titanium layer and Si atom in the polysilicon layer 34A. Next, wet etching process is performed to remove the Ti layer remaining on the second insulating layer 33 and the $TiSi_x$ layer.

As shown in FIG. 3D, a part of the diffusion barrier layer 34C is etched using an etchant, such as a mixed gas comprising Cl_2 and BCl_3, to which the diffusion barrier layer 34C has a higher etching selectivity than the second insulting layer 33.

As shown in FIG. 3E, a seed layer 34D is deposited on the second insulating layer 33 and the diffusion barrier layer 34C.

A blanket etching process or a CMP process is performed until the second insulating layer 33 is exposed. Thereby, the plug 34, composed of polysilicon layer 34A, the ohmic contact layer 34B, the diffusion barrier 34C and the seed layer 34D, are completely formed. In the present invention, Ru, Ir, Pt, SrO, W, Mo, Co, Ni, Au or Ag is deposited by using a chemical vapor deposition technique, for forming the seed layer 34D.

Also, the process for forming the polysilicon layer 34A may be omitted, in such a case, the plug 34 is composed of the ohmic contact layer 34B layer, the diffusion barrier layer 34C and the seed layer 34D. Moreover, the process for forming the ohmic contact layer 34B may be omitted, in such a case, the plug 34 is composed of the polysilicon layer 34A, diffusion barrier layer 34C and the conducting layer 34D. Accordingly, it is possible that the plug 34 is composed of the diffusion barrier layer 34C and the conducting layer 34D.

As shown in FIG. 3F, a glue layer 35 is formed on the seed layer 34D and the second insulating layer 33. Thereafter, a sacrificial layer 36 is formed on the glue layer 35. In the present invention, the glue layer 35 is formed with TiN, TiAlN, TaN, TaSiN, Al_2O_3 or TiO_2 50 - 500 Å thick, and the sacrificial layer 36 is formed with silicon oxide to a thickness of 5000 - 15000 Å.

As shown in FIG. 3G, the sacrificial layer 36 and the glue layer 35 are selectively etched to form an opening exposing the seed layer 34D. A lower electrode 37 is formed on the seed layer 34D in the opening. In the present invention, a Pt layer, as the lower electrode 37, is deposited to a thickness of 4000 - 12000 Å by electroplating. A current density of 0.1 - 20 mA/cm^2 is imposed on the conducting layer 31, with DC or a DC pulse. On the other hand, the semiconductor substrate 30 may be used as an electrode during the electro plating, in case the conducting layer 31 is not formed.

As shown FIG. 3H, the sacrificial layer 36 and the glue layer 35 are removed by wet etching using an HF solution or BOE solution. Also, the glue layer 35 may be removed by using dry etching.

According to the preceding process of the present invention, the diffusion barrier layer 34C of the plug 34 is not exposed, even if the mask misalignment has occurred in the process for forming the opening. That is, the seed layer 34D, covering the diffusion layer 34C, is exposed in the case of the occurring mask misalignment.

As shown in FIG. 3I, a dielectric layer 38 is deposited on the lower electrode 37 and the second insulating layer 33. Thereafter, an upper electrode 39 is formed on the dielectric

layer 38. In the present invention, a BST layer is deposited to a thickness of 150 - 500 Å and at a temperature of 350 - 600 °C for forming the dielectric layer 38. An annealing process, for crystallizing the dielectric layer 38, is performed in an N_2 gas atmosphere at a temperature of 500 - 700 °C for 30 - 180 seconds, thereby the dielectric characteristic of the dielectric layer 28 may be improved. The upper electrode 39 is formed with a material, such as Pt, Ru, Ir or SrO.

There are several advantages to forming the conducting layer on the diffusion barrier. A first advantage is that it is possible to prevent the dielectric layer being contacted with the diffusion barrier. A second advantage is that it is possible to reduce the leakage current. A third advantage is that it is possible to prevent the diffusion barrier from being exposed even if mask misalignment has occurred, thereby the annealing for crystallizing the dielectric layer may be performed at a high temperature. A fourth advantage is that it is possible to obtain high capacitance of the capacitor in the highly integrated semiconductor device.

Although the one preferred embodiment of the invention has been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and

spirit of the invention as disclosed in the accompanying claims.

SEMICONDUCTOR MEMORY DEVICE HAVING A PLUG CONTACTED TO A CAPACITOR ELECTRODE AND METHOD FOR FABRICATING THE [SAME] CAPACITOR

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method for fabricating a semiconductor memory device; and more particularly, to a method for fabricating a capacitor of a semiconductor memory device.

Description of the Prior Art

A DRAM (Dynamic Random Access Memory) cell is a semiconductor memory device typically comprising of one transistor and one capacitor, in which one bit of data is stored in a cell by using an electric charge. A capacitor comprises of a lower electrode, a dielectric layer, and an upper electrode. One electrode of the capacitor is connected to the source/drain junction of the transistor. Another electrode of the capacitor is connected to a reference voltage line.

Advances in computer applications have increased the demand for higher capacity memory chips. [Decreasing] By decreasing the size of the memory cells, [allows] more memory cells [to] can be packed into an integrated circuit.

The capacitance of a capacitor is proportional to the

surface area of the electrodes and a dielectric constant of a dielectric layer. As the area of the memory cell has decreased, the capacitance of the [capacitors] capacitor tends to decrease. [also, lowering] This lowers the performance of the memory cells.

In order to increase the density of the memory cells, stacked capacitors have been proposed. Stacked capacitors are formed by partially stacking the storage electrode over the transistor and over the bit/word line, thereby effectively reducing the area used for each memory cell.

A plug is used to connect the lower electrode of the capacitor with the source/drain junction of the transistor.

A method for fabricating a capacitor of a semiconductor memory device according to the conventional method is described by referring to FIG. 1A to FIG. 1C.

As shown in FIG. 1A, an insulating layer 15 is formed over a semiconductor substrate 10, an isolation layer 11, such as field oxide layer, and a transistor comprising a gate insulating layer 12, a gate electrode 13 and the source/drain junctions 14. Thereafter, a plug 16 is formed in the interlayer insulating layer. The plug 16 is composed of a [ploysilicon] polysilicon layer 16A, an ohmic contact layer 16B and a diffusion barrier layer 16C formed in a contact hole,

exposing one of [the] a source/drain junctions 14.

As shown in FIG. 1B, a lower electrode 17 is formed on the diffusion barrier layer 16C by depositing and patterning a first conductive layer. The diffusion barrier layer 16C may be exposed during the formation of the lower electrode 17 because of a mask misalignment. The mask misalignment [is] frequently [occurred] occurs in [a] the manufacturing process of [a] the highly integrated device.

As shown in FIG. 1C, a dielectric layer 18 is formed on the lower electrode 17 and an upper electrode 19 is formed on the dielectric layer 18. The dielectric layer 18 is formed with a material exhibiting a very high dielectric constant, such as Barium [strontium titanate] Strontium Titanate ($BaSrTiO_3$, hereafter abbreviated BST), to increase the capacitance in a highly integrated device.

The present invention relates to a method for fabricating a semiconductor memory device; and more particularly, to a method for fabricating a capacitor of a semiconductor memory device.

An electro plating technique is used to form the lower electrode without an etching process.

A method for fabricating a capacitor of a semiconductor memory device according to a second conventional method, by

using the electro plating technique, is described by referring to FIG. 2A to FIG. 2E.

As shown in FIG. 2A, an insulating layer 15 is formed over a semiconductor substrate 10, an isolation layer 11, such as a field oxide layer, and a transistor comprising a gate insulating layer 12, a gate electrode 13 and source/drain junctions 14. Thereafter, a plug 16 is formed in the insulating layer. The plug 16 is composed of a [ploysilicon] polysilicon layer 16A, an ohmic contact layer 16B and a diffusion barrier layer 16C formed in a contact hole, exposing one of the source/drain junctions 14.

As shown in FIG. 2B, a seed layer 21 is formed on the insulating layer 15 and the plug 16, thereafter a glue layer 22 and a sacrificial layer 23 are stacked, one by one, on the seed layer 21.

As shown in FIG. 2C, the sacrificial layer 23 and the glue layer 22 [is] are selectively etched to form an opening exposing the seed layer 21[, and a]. A lower electrode 17 is formed on the seed layer 21 in the opening.

As shown in FIG. 2D, the sacrificial layer 23, the glue layer 22 and the seed layer 21 are removed to separate the neighboring [the] lower electrodes 17.

As shown in FIG. 2E, a dielectric layer 18 is deposited on

the lower electrode 17 and the insulating layer 15. Thereafter, an upper electrode 19 is formed on the dielectric layer 18.

In the [preceding] mentioned process of the second conventional method, the diffusion barrier layer 16C of the plug 16 may be exposed after removing the seed layer 21 when [the] mask misalignment [is] has occurred in the process for forming the opening.

According to the [above] stated conventional method, the exposed part of the diffusion barrier layer 16C of the plug 16 is contacted to the dielectric layer 18.

There are several problems [generated] caused by the contact between the diffusion layer 16C and the dielectric layer 18. One problem is that the diffusion barrier layer 16C is oxidized during the process for forming the dielectric layer 18, because the dielectric layer 18, [such as the BST layer], is formed under an oxygen gas atmosphere and at a high temperature. The oxidized part of the diffusion barrier layer 16C, exhibiting low dielectric constant, plays [a] the role of [a] the dielectric layer of [a] the capacitor, thereby the capacitance of the capacitor is reduced. The other problem is that the work function difference, between the diffusion barrier 16C and the dielectric layer 18, is low[, thereby]. Thus, the leakage current is increased, because of the low

Schottky barrier height.

[Summary of the Invention] **SUMMARY OF THE INVENTION**

It is, therefore, an object of the present invention to provide a semiconductor memory device and a fabrication method capable of preventing [the] contact between a dielectric layer of a capacitor and a diffusion barrier of a plug.

It is, therefore, another object of the present invention to provide a semiconductor memory device and a fabrication method capable of preventing [the] a lowering of the capacitance of [a] the capacitor and [the increasing] an increase of the leakage current between the lower electrode of [a] the capacitor and a diffusion barrier of a plug.

In accordance with an aspect of the present invention, there is provided a semiconductor memory device, comprising[:] a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein source/drain junctions are formed in the semiconductor substrate[; an]. An interlayer insulating layer is formed over the semiconductor substrate[;]and a plug is formed in the interlayer insulating layer[, wherein the]. The plug comprises a diffusion barrier layer and a seed layer for a electro plating[; a]. A lower electrode of the capacitor is contacted

to the seed layer[; a]. A dielectric layer is formed on the lower electrode[;] and an upper electrode is formed on the dielectric layer.

In accordance with another aspect of the present invention, there is provided a method for fabricating semiconductor memory device[, comprising]. The method includes the steps of[:] providing a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein source/drain junctions are formed in the semiconductor substrate[;], and forming an interlayer insulating layer over the semiconductor substrate[; etching the]. The interlayer insulating layer is etched to form a contact hole[;]. [forming a] A plug is formed in the contact hole[, wherein the]. The plug comprises a diffusion barrier layer and a seed layer for [a] electro plating[; forming a]. A lower electrode of a capacitor is formed and is contacted to the seed layer by using [an] the electro plating technique[; forming] Also, a dielectric layer of the capacitor is formed on the lower electrode[;] and [forming] an upper electrode of the capacitor is formed on the dielectric layer.

In accordance with still further [another] aspect of the present invention, there is a method for fabricating semiconductor memory device[, comprising]. The method includes

the steps of[:] providing a semiconductor substrate, wherein a gate electrode is formed on the semiconductor substrate, and wherein a plurality of source/drain junctions are formed in the semiconductor substrate[;] and forming an interlayer insulating layer over the semiconductor substrate[; etching the]. The interlayer insulating layer is etched to form a contact hole[; forming a]. A plug is formed in the contact hole, wherein the plug comprises a diffusion barrier layer and a seed layer for [a] electro plating[; forming a]. A glue layer is formed on the seed layer and the interlayer insulating layer[; forming a]. A sacrificial layer is formed on glue layer[; etching the]. The sacrificial layer and the glue layer are etched to form an opening defining a region of a lower electrode of a capacitor[; forming the]. The lower electrode is formed on the seed layer in the opening, by using [an] the electro plating technique[; removing the]. The sacrificial layer and the glue layer are removed. A [; forming a] dielectric layer of the capacitor is formed on the lower electrode[;] and [forming] an upper electrode of the capacitor is formed on the dielectric layer.

[Brief Description of the Drawings] **BRIEF DESCRIPTION OF THE DRAWINGS**

The above and other objects and features of the present invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

FIG. 1A to FIG. 1C are cross sectional views showing a method for fabricating a semiconductor memory device according to a first conventional method.

FIG. 2A to FIG. 2E are cross sectional views showing a method for fabricating a semiconductor memory device according to a second conventional method.

FIG. 3A to FIG. 3I are cross sectional views showing a method for fabricating a capacitor of a semiconductor device according to [an embodiment of] the present invention.

[Detailed Description of the Preferred Embodiments] **DESCRIPTION OF THE INVENTION**

Hereinafter, a semiconductor memory device fabrication method according to [embodiments of] the present invention will be described in detail referring to the accompanying drawings.

As shown in FIG. 3A, a conducting layer 31 is formed over a semiconductor substrate 30[, on which a]. A determined lower structure (not shown), [comprising] comprises an isolation

layer, such as a field oxide layer, a transistor including a gate insulating layer, a gate electrode and the source/drain junctions. Thereafter, an interlayer insulating layer, composed of a first insulating layer 32 and a second insulting layer 33, is formed on the conducting layer 31.

The conducting layer 31 is used as an electrode for forming a lower electrode of a capacitor, by using [an] electro plating technique. In the [preferred embodiment of the] present invention, a doped polysilicon layer is deposited and a thermal treatment process is performed to activate impurities in the doped polysilicon layer, whereby the conducting layer 31 is formed.

The process for forming the conducting layer 31 may be omitted, in this case, and the semiconductor substrate 30 may be used as the electrode for forming a lower electrode of a capacitor. The second insulating layer 33, playing as an antireflection layer, is formed with a material of which etching is selectivity [is] higher than the first insulating layer 32. In [a preferred embodiment of] the present invention, the first insulating layer 32 is formed by depositing a silicon oxide layer to a thickness of 3000 - 8000 Å, and the second insulating layer 33 is formed by depositing a silicon nitride layer to a thickness of 300 to 1000 Å.

As shown in FIG. 3B, the second insulating layer 33 and the first insulating layer 32 are etched to form a contact hole exposing the conducting layer 31. One of the source/drain [junction] junctions (not shown) formed in the semiconductor substrate 30 may be exposed by the contact hole, if the conducting layer 31 is not formed.

And then, a polysilicon layer 34A, for forming a plug, is deposited to a thickness of 500 - 3000 Å on the second insulating layer 33 and in the contact hole. Thereafter, an etching process is performed to expose the surface of the second insulting layer 33 and to remove a part of the polysilicon layer 34A in the contact hole. Thereby, the height difference between the surface of the second insulating layer 33 and the surface of the polysilicon layer 34A becomes 500 to 1500 Å.

As [sown] shown in FIG. 3C, an ohmic contact layer 34B and a diffusion barrier layer 34C are formed, one by one, on the polysilicon layer 34A. Subsequently, a chemical mechanical polishing (hereafter, abbreviated CMP) process is performed until the surface of the second insulating layer 33 is exposed. In [a preferred embodiment of] the present invention, the ohmic contact layer 34B is formed with $TiSi_x$ and the diffusion barrier layer 34C is formed with TiN, TiSiN, TiAlN, TaSiN, TaAlN, IrO_2 or RuO_2. For forming the $TiSi_x$, a Ti layer is deposited, an

annealing process is performed for a reaction between Ti atom in the titanium layer and Si atom in the polysilicon layer 34A[, and a wet]. Next, wet etching process is performed to remove the Ti layer remaining on the second insulating layer 33 and the $TiSi_x$ layer.

As shown in FIG. 3D, a part of the diffusion barrier layer 34C is etched using an etchant, such as a mixed gas comprising Cl_2 and BCl_3, to which the diffusion barrier layer 34C has a higher etching selectivity than the second insulting layer 33.

As shown in FIG. 3E, a seed layer 34D is deposited on the second insulating layer 33 and the diffusion barrier layer 34C[, and a]. A blanket etching process or a CMP process is performed until the second insulating layer 33 is exposed. Thereby, the plug 34, composed of polysilicon layer 34A, the ohmic contact layer 34B, the diffusion barrier 34C and the seed layer 34D, [is] are completely formed. In the [preferred embodiment of] the present invention, Ru, Ir, Pt, SrO, W, Mo, Co, Ni, Au or Ag is deposited by using a chemical vapor deposition technique, for forming the seed layer 34D.

Also, the process for forming the polysilicon layer 34A may be omitted, in such a case, the plug 34 is composed of the ohmic contact layer 34B layer, the diffusion barrier layer 34C and the seed layer 34D. Moreover, the process for forming the ohmic

contact layer 34B may be omitted, in such a case, the plug 34 is composed of the polysilicon layer 34A, diffusion barrier layer 34C and the conducting layer 34D. Accordingly, it is possible that the plug 34 is composed of the diffusion barrier layer 34C and the conducting layer 34D.

As shown in FIG. 3F, a glue layer 35 is formed on the seed layer 34D and the second insulating layer 33[, thereafter]. Thereafter, a sacrificial layer 36 is formed on the glue layer 35. In the [preferred embodiment of the] present invention, the glue layer 35 is formed with TiN, TiAlN, TaN, TaSiN, Al_2O_3 or TiO_2 50 - 500 Å thick, and the sacrificial layer 36 is formed with silicon oxide to a thickness of 5000 - 15000 Å [thick].

As shown in FIG. 3G, the sacrificial layer 36 and the glue layer 35 [is] are selectively etched to form an opening exposing the seed layer 34D[, and a]. A lower electrode 37 is formed on the seed layer 34D in the opening. In the [preferred embodiment of the] present invention, a Pt layer, as the lower electrode 37, is deposited to a thickness of 4000 - 12000 Å by [the] electroplating. A current density of 0.1 - 20 mA/cm^2 is imposed on the conducting layer 31, with DC or a DC pulse. On the other hand, the semiconductor substrate 30 may be used as an electrode during the electro plating, in case the conducting layer 31 is not formed.

As shown FIG. 3H, the sacrificial layer 36 and the glue layer 35 are removed by [a] wet etching using an HF solution or BOE solution. Also, the glue layer 35 may be removed by [a] using dry etching.

According to the preceding process of the present invention, the diffusion barrier layer 34C of the plug 34 is not exposed, even if the mask misalignment [is] has occurred in the process for forming the opening. That is, the seed layer 34D, covering the diffusion layer 34C, is exposed in the case of the occurring [the] mask misalignment.

As shown in FIG. 3I, a dielectric layer 38 is deposited on the lower electrode 37 and the second insulating layer 33. Thereafter, an upper electrode 39 is formed on the dielectric layer 38. In the [preferred embodiment of the] present invention, a BST layer is deposited to a thickness of 150 - 500 Å and at a temperature of 350 - 600 °C for forming the dielectric layer 38[, and an]. An annealing process, for crystallizing the dielectric layer 38, is performed in an N_2 gas atmosphere at a temperature of 500 - 700 °C for 30 - 180 seconds, thereby the dielectric characteristic of the dielectric layer 28 may be improved. The upper electrode 39 is formed with a material, such as Pt, Ru, Ir or SrO.

There are several advantages to [form] forming the

[conducing] conducting layer on the diffusion barrier. A first advantage is that it is possible to prevent the dielectric layer being contacted with the diffusion barrier. A second advantage is that it is possible to reduce the leakage current. A third advantage is that it is possible to prevent the diffusion barrier from being exposed even if [the] mask [misalign is] misalignment has occurred, thereby the annealing for crystallizing the dielectric layer may be performed at a high temperature. A fourth advantage is that it is possible to obtain high capacitance of the capacitor in the highly integrated semiconductor device.

Although the one preferred [embodiments] embodiment of the invention [have] has been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.